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Design Analysis of Dickson Charge Pump in 90nm Technology

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Abstract: **This paper represents the analysis of 6 stage Dickson charge pump. The aim is to compare the current, efficiency, voltage of Dickson charge pump using either diodes or MOSFET's as diodes. This paper presents the suitable criteria for properly sizing the capacitors according to clock signals, which allows the charge pump performance to be optimized. A six-stage Dickson charge pump was designed to produce a 7.36 V output from a 1.2V supply, using 250 kHz, two-phase non-overlapping clock signal driving the charge pump.**

Keywords: **high voltage DC output; DC-DC converter; charge pump; single clock charge pump; Dickson charge pump.**

I. INTRODUCTION

The electronics world is being attracted by the mobile or portable devices like laptops, mobile phones and portable measurement instruments. In these applications average power consumption becomes crucial. Low power consumption or efficient circuit designs play a key role in these portable applications. Low power and low voltage applications are becoming more important but these low voltage applications still need higher voltages to drive internal circuits such as flash memory or EEPROM [1]. For this purpose the supply or battery voltage could not be scaled up, due to size and weight constraints of portable devices. Therefore it is important to use an efficient charge pump to increase the voltage of power supply up to required level, to meet power requirement of portable devices.

Basically, a CP is a capacitor network providing a voltage gain G (defined as the ratio between the open-circuit output voltage VOUT, max and the input voltage VDD) and having an equivalent output resistance R_{OUT}, which depends on the topology frequency f and the size of capacitors C_{ST} [2], [3]. Charge pumps usually operate at a high- frequency level in order to increase their output power within a reasonable size of total capacitance used for charge transfer. This operating frequency may be adjusted by [4] compensating for changes in the power requirements and saving the energy delivered to the charge pump.

Among many approaches to the charge pump design, the switched-capacitor circuits such as Dickson charge pump [4] are very popular, because they can be implemented on the same chip together with other components of an integrated system.

Due to the efficiency consideration, the switching type DC converter is rather preferred; and for low power applications, the switched-capacitor (SC) converters are usually the first choice owing to their [4] advantages of lower costs and less area occupied. The Dickson charge pump is appropriate for [1] on chip fabrication. Dickson charge pump uses diode associated MOS transistors and a series of capacitors driven by two complementary clocks to transfer charges from the power supply to the load capacitor at a higher voltage. The main drawback is the threshold voltage drop related by means of the diode connected transistors.

II. COCKCROFT-WALTON VOLTAGE MULTIPLIER

The first widely used voltage boosting circuit was the Cockcroft-Walton voltage multiplier [5]. This circuit, shown in Fig. 1, uses diodes and serially connected capacitors and can boost to several times the supply voltage. The Cockcroft-Walton

charge pump provides efficient multiplication only if the coupling capacitors are much larger than the stray capacitance in the circuit, making it undesirable for use in integrated circuits.

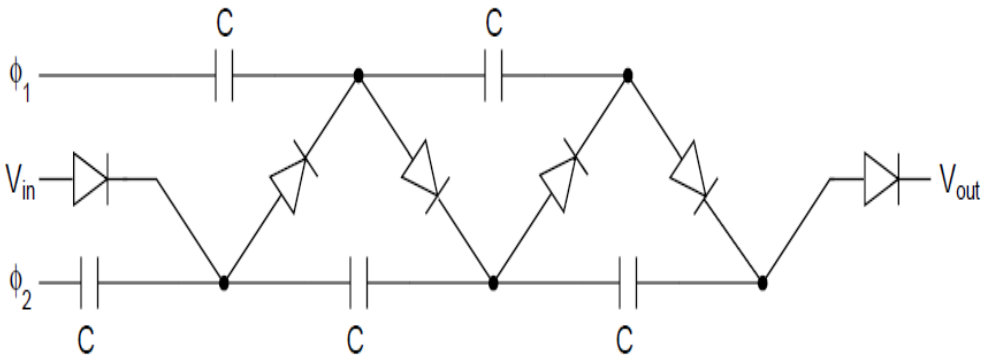

Fig.1. 5-stage Cockcroft-Walton charge pump

III. DICKSON CHARGE PUMP

The Dickson charge pump circuit is presented as an improvement of Cockcroft-Walton circuit. [6] In the Cockcroft-Walton charge pump circuit, the coupling capacitors are connected in series. This results in high output impedance as the number of stages increases. In the Dickson charge pump circuit, shown in Fig. 2, the coupling capacitors are connected in parallel and must be able to withstand the full output voltage. This results in low output impedance as the number of stages increases. Both circuits require the same number of diodes and capacitors and can be shown to be equivalent. The drawback of the Dickson charge pump circuit is that the boosting ratio is degraded by the threshold drops across the diodes.

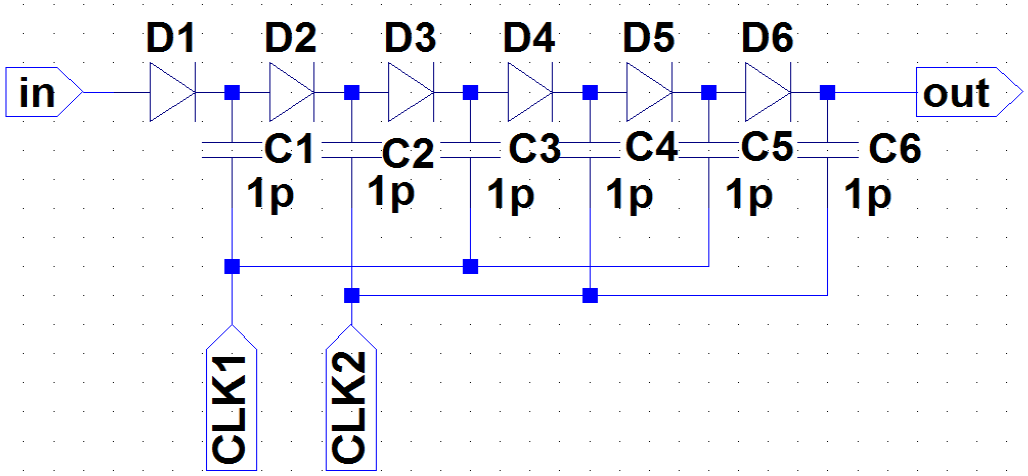

Fig.2. 6-stage Dickson charge pump

The Dickson Charge pumps were designed to generate high voltage much greater than the supply voltage [2] from which they operate. The Dickson charge pump circuit consists of two clock inputs i.e. CLK and CLK, which are opposite in phase. The diodes operate as self-timed switches characterized by a forward bias voltage (V_{df}) and the clock amplitude. The Dickson charge pump, boost up the voltage along the diode chain as the capacitor of each stage charge and discharge alternatively, reference to the clock amplitude during the each clock cycle. Initially, when clock CLK goes low, diode D1 conducts until the voltage at node 1 i.e. V1 becomes:

$V1 = V_{in} - V_{df}$ (1)

V_{df} is diode's threshold voltage. When CLK is switched, the voltage at node 1 now becomes:

$V1 = V_{in} + V_{in} - V_{df}$ (2)

Since, amplitudes of V_{in}, and both clock inputs are equal. At the same time CLK goes low, which causes diode D2 to conduct until the voltage at node 2 i.e. V2 becomes:

$V2= (V_{in} + \overline{V}_{in} - V_{df}) - V_{df}$ (3)

When CLK goes high again, the voltage at node 2 becomes:

$V2= V_{in} + 2(V_{in} - V_{df})$ (4)

After N stages, it is easy to see that the output voltage is

$V_{out} = V_{in} + N(V_{in} - V_{df})$ (5)

Effect of stray capacitance is being ignored here. In presence of load, the output voltage is given by

$$V_{out} = V_{in} + N\left[V_{in} - V_{df} - \frac{I_{out}}{2*pi*C.f_{osc}}\right] \quad (6)$$

At no load, the term

"$I_{out}/2 * pi * C.f_{osc}$" becomes zero and we get the equation (5) again. "f_{osc}" could be calculated by the given formula [2], i.e.

$$f_{osc} = \frac{I_{out}N}{C.\Delta V_{tot}} \quad (7)$$

Where "ΔV_{tot}" could be calculated as:

$$\Delta V_{tot} = (N+1)(V_{in} - V_{df}) - V_{out} \quad (8)$$

A Dickson charge pump circuit is constructed practically shown as fig. 2, using six diodes for six number of stages, six 1pf capacitors, two clock inputs of 250kHz with an amplitude of 1.2 V and the supply voltage Vin =1.2 volts.

IV. DICKSON CHARGE PUMP USING MOSFET'S

The six stages block diagram of Dickson Charge pump is shown in fig. 3. The basic cell, behind the blocks of Dickson charge pump, is [1] shown in fig. 4. The PMOS transistor used with bulk terminal connected to source i.e. V_{sb}=0, to charge the capacitor of each stage.

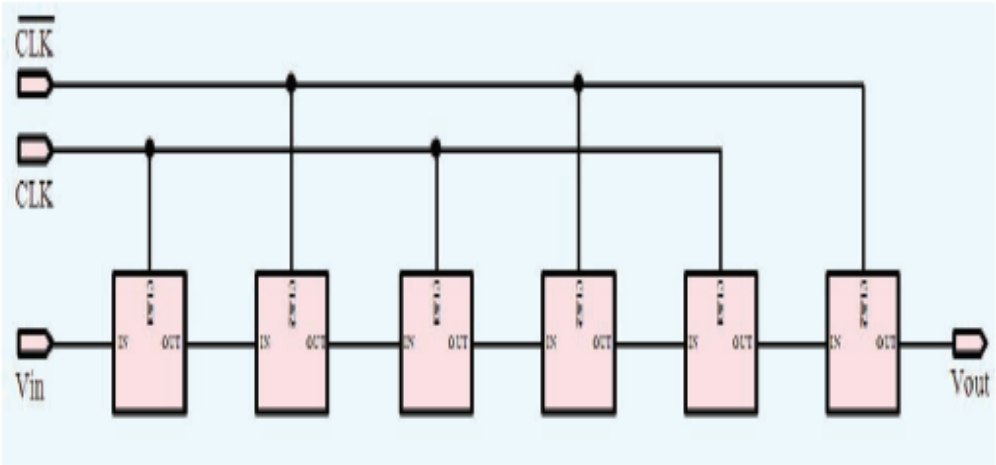

Fig.3. Dickson Charge Pump Block Diagram

The MOSFET charge transfer switch (CTS) connection used in the charge pump is implemented by connecting the gate (G), source (S), and body (B) together. In this implementation, the floating-body of the p-channel is connected to the source, thus shorting the junction from the n-type body to the p-type source. Hence, only one diode exists between the gate-source-body connection and the [1] drain. In this configuration the gate-source-body connection will serve as the anode and the drain as the cathode. Hence it will work as a diode and will be having lesser threshold voltage V_{th}. Such as for lower voltages it would be 0V. Basic circuit is shown below in fig.4.

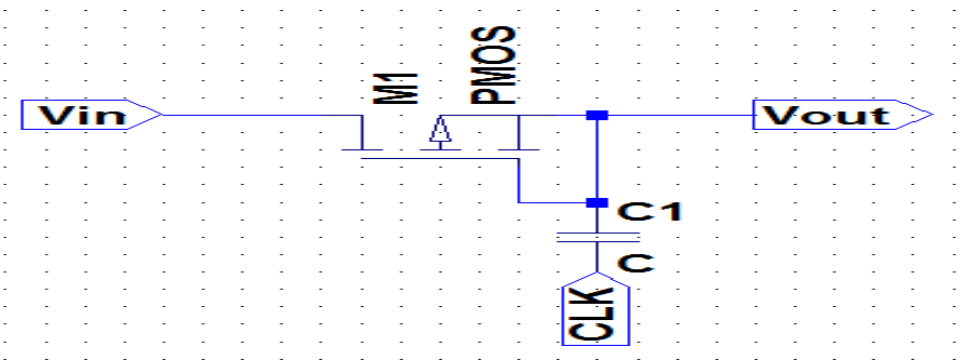

Fig.4. Dickson Charge Pump Basic Block

The configuration shown in fig. 3 is used to generate higher voltage with V_{in} along with two 180° out of phase clock pulses having 50% duty cycle. It can be seen in fig. 3 that PMOS transistor is used in diode connected configuration with bulk of the transistor [1] is connected to the source and gate, so the maximum voltage gain V_g per stage of the Dickson charge pump circuit can be calculated as

$$Vg = V_{in} - V_t \quad \text{(i)}$$

Where V_t is the threshold voltage of the PMOS transistor. As shown in fig. 2 and fig. 3, the Dickson charge pump is developed by diode connected PMOS transistors instead of diodes. Therefore V1, V2, or V_{out} can be calculated by replacing V_{df} with the threshold voltage "V_t" of PMOS [1] from the above equations (1) to (8).

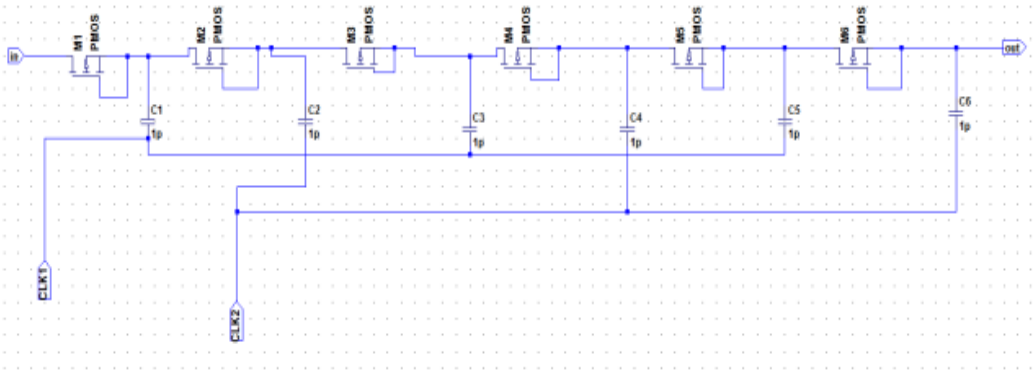

Fig.5. Dickson charge pump using MOSFET's

V. DICKSON CHARGE PUMP USING SINGLE CLOCK

Two non-overlapping clocks are needed in the Dickson charge pump to prevent clock feed through. The circuit used here requires one clock signal input and generates a two-phase non-overlapping clock [7]. The amount of overlap is determined by the delay through the NOR gate and the buffer on the NOR gate output. When the input clock goes high, this forces clk1 low and subsequently forces clk2 high. When the input goes low, clk2 becomes low. Only after clk2 goes low, clk1 can go high. Buffers are required at the output of the two non-overlapping clocks in order to drive the capacitors at each stage.

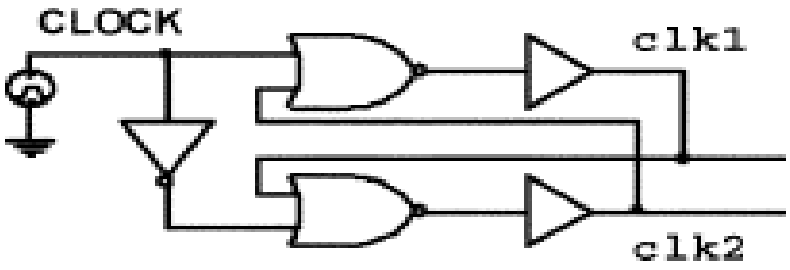

Fig.6. Non-overlapping clock generator

The power loss in the charge pump circuit is composed of two parts; one is the resistive power loss (also called conduction loss) and the other is the dynamic power loss (also called switching loss). To improve the charge pump's efficiency, there are two circuit parameters that must be optimized: the switching frequency and the on-state conductance of the body diode. The switching frequency is controlled by the selection of the clock frequency, and the on-state resistance is controlled by the design of the CTS. There is an optimal value for switching frequency so that the power loss is minimized, i.e., the [7] efficiency is maximized.

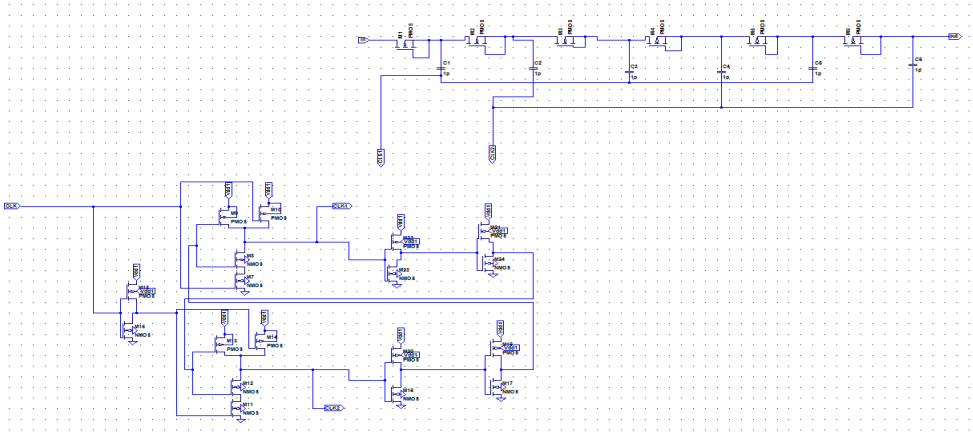

Fig.7. Dickson charge pump using Non-overlapping clock generator.

A higher switching frequency lowers the efficiency due to the increased switching losses. If the frequency is too low, one observes conduction losses as a limiting factor (Fig. 6). At a certain point, the efficiency peaks. The simulation results in the efficiency increases. This occurs until the clock frequency reaches about 4 MHz's when the clock frequency is increased further, the efficiency decreases. The authors chose a 4 MHz clock to achieve peak efficiency [7]. The efficiency at 4MHz is slightly higher than 5 MHz, but either choice would provide approximately 79% efficiency. In fact, to guard against a frequency shift, 5 MHz would be a more suitable choice.

VI. DICKSON CHARGE PUMP VARIATION SUPPERSSION

As all of the above circuits are having variations at output so to make it as stable output used one more switch and a capacitor which is grounded at the output point as shown in fig.7 below.

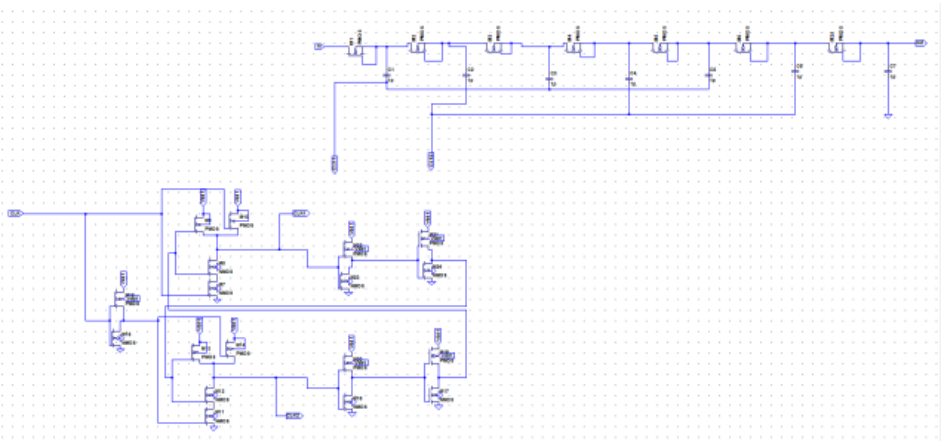

Fig.8. Dickson charge pump variations suppressed

VII. DICKSON CHARGE PUMP SIMULATIONS

For all the above circuits transient analysis is shown for 7000us.

Dickson charge pump simulation is shown below in the fig.. It is the basic Dickson charge pump using diodes having some threshold voltage V_{th}, input dc voltage as 1.2V and clocks of opposite phases having characteristics as voltage

amplitude levels 0V to 1.2V and having pulse width as 2us and period as 4us. As the transient analysis shows output voltage variations as from 4.15V to 5.35V.

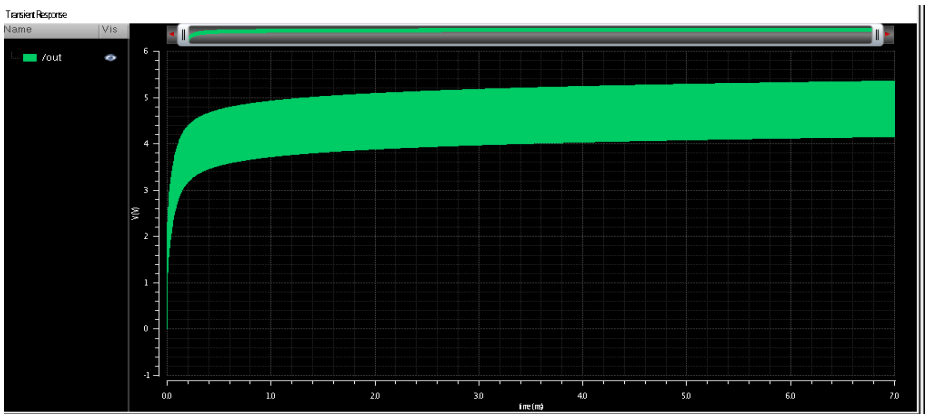

Fig.9. Transient analysis of Dickson charge pump.

Dickson charge pump variation suppressed simulation is shown below in the fig.. It is the basic Dickson charge pump using diodes having some threshold voltage V_{th}, input dc voltage as 1.2V and clocks of opposite phases having characteristics as voltage amplitude levels 0V to 1.2V and having pulse width as 2us and period as 4us. As the transient analysis shows output voltage as 4.77V. To make output as stable output used one more switch and a capacitor which is grounded at the output point.

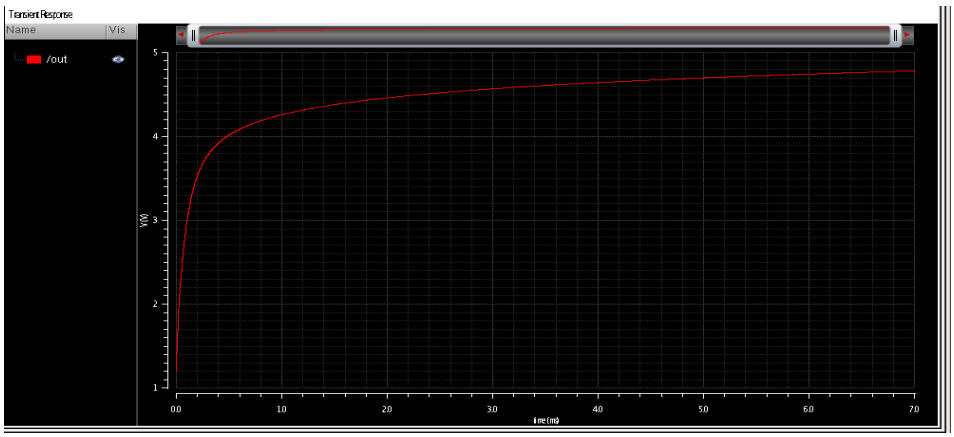

Fig.10. Transient analysis of Dickson charge pump variations suppressed.

Dickson charge pump using MOSFET's simulation is shown below in the fig.. It is the Dickson charge pump using MOSFET's as a diode, input voltage as 1.2V and clocks of opposite phases having characteristics as voltage amplitude levels 0V to 1.2V and having pulse width as 2us and period as 4us. As the transient analysis shows output voltage variations as from 6.24V to 7.44V.

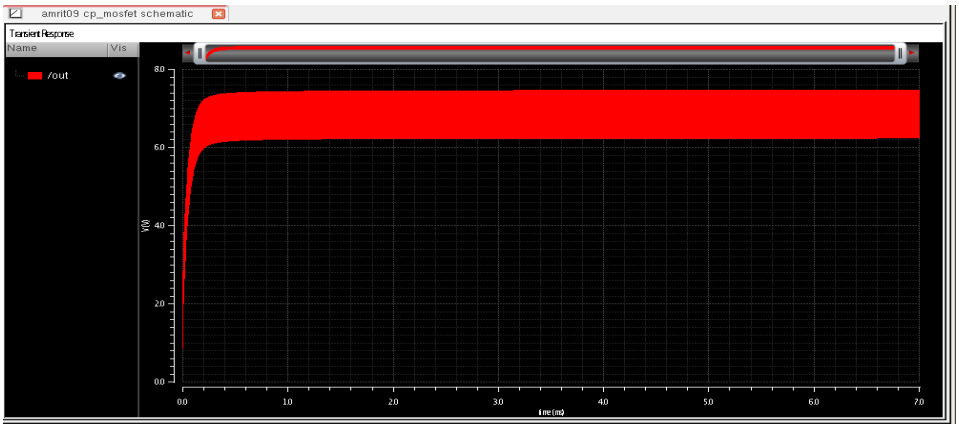

Fig.11. Transient analysis of Dickson charge pump using MOSFET's as diodes.

Dickson charge pump using MOSFET's as diodes with single clock using non-overlapping clock generator simulation is shown below in the fig. It is the Dickson charge pump using MOSFET's as diodes, input dc voltage as 1.2V and only 1 clock having characteristics as voltage amplitude level 0V to 1.2V and having pulse width as 2us and period as 4us and Vdd1 having 1.2V. As the transient analysis shows output voltage variations as from 6.24V to 7.44V.

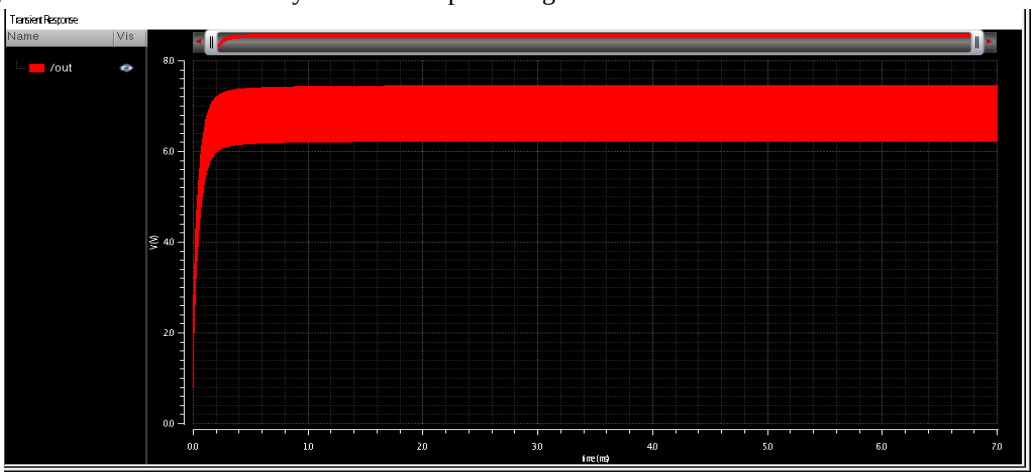

Fig.12. Transient analysis of Dickson charge pump using MOSFET's as diodes with single clock using non-overlapping clock generator.

Dickson charge pump using MOSFET's as diodes with single clock using non-overlapping clock generator and variations suppressed simulation is shown below in the fig.. It is the Dickson charge pump using MOSFET's as diodes, non-overlapping clock generator and variations are suppressed using 1 extra MOSFET as a switch and 1 capacitor connected to ground, input dc voltage as 1.2V and only 1 clock having characteristics as voltage amplitude level 0V to 1.2V and having pulse width as 2us and period as 4us and Vdd1 having 1.2V. As the transient analysis shows output voltage is 7.36V.

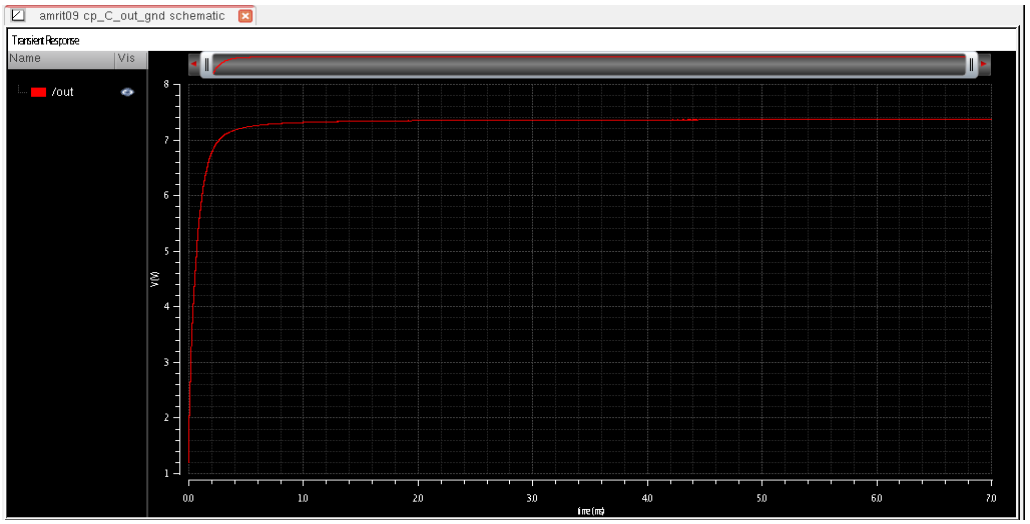

Fig.13. Transient analysis of Dickson charge pump using MOSFET's as diodes with single clock using non-overlapping clock generator and variations suppressed.

Efficiency calculation

$$\eta = \frac{\frac{V_{out}}{V_{in}}}{N + 1 + \alpha . \frac{N^2}{N + 1 - \frac{V_{out}}{V_{in}}}} . 100$$

The α parameter is technology dependent, varying between 0.1 (for poly-poly capacitors) and 0.4 (for other capacitors like metal-metal capacitors)

VII. COMPARISION

Configuration (input voltage=1.2)	Output voltage (V)	Current (Load resistance 100MΩ)	Efficiency (%)
COCKCROFT-WALTON VOLTAGE MULTIPLIER	4.22	22nA	50
DICKSON CHARGE PUMP using diodes	5.35	27nA	53
DICKSON CHARGE PUMP using MOSFET's	7.36	55nA	56

REFERENCES

[1] Muhammad Adeel Ansari, Waqar Ahmad, Svante R. Signell, (June 2011). Single clock charge pump designed in 0.35µm technology, IEEE MIXDES 2011, 18th International Conference "Mixed Design of Integrated Circuits and Systems", Gliwice, Poland, pp 552-555.

[2] J. F Dickson, "on chip high voltage generation in NMOS integrated circuits using an improved voltage multiplier technique", IEEE J. Of Solid-State Circuits, vol. 11, no. 3, pp. 374-378, June 1976.

[3] T. Tanzawa and T. Tanaka, "A dynamic analysis of the Dickson charge pump circuit", IEEE J. of Solid-State Circuits, vol. 32, no. 8, pp. 1231-1240, Aug. 1997.

[4] Janusz A. Starzyk, Senior Member, IEEE, Ying-Wei Jan, and Fengjing Qiu, (MARCH 2001). A dc–dc charge pump design based on voltage doublers, IEEE transactions on circuits and systems—i: fundamental theory and applications, vol. 48, no. 3, pp 350-359.

[5] J. D. Cockcroft and E. T. Walton, "Production of high velocity positive ions," Proceedings of the Royal Society of London, A, vol. 136, pp. 619-630, 1932.

[6] J. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," IEEE Journal of Solid-State Circuits, vol. SC-11, pp. 374-378, June 1976.

[7] M. R. Hoque, T. Ahmad, Member, IEEE, T. R. McNutt, Member, IEEE, H. A. Mantooth, Senior Member, IEEE, and M. M. Mojarradi, Member, IEEE, (MAY 2006). A technique to increase the efficiency of high-voltage charge pumps, IEEE transactions on circuits and systems—ii: express briefs, vol. 53, no. 5, pp 364-368.